REMARKS

Claims 1-28 are pending in the present application. In the Office Action dated March 24, 2006, claims 1, 4, 5-8, 10, 12-14 and 18-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,084,838 to Kajimoto et al. ("Kajimoto"). Claim 22 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No. 2004/0024959 to Taylor ("Taylor"). Claims 2, 11 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kajimoto et al. in view of U.S. Patent No. 3,355,725 to McKeon ("McKeon"). Claims 3, 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kajimoto et al. in view of U.S. Patent No. 6,667,873 to Lyke et al. ("Lyke"). Claims 23-26 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Taylor in view of McKeon. Claim 27 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Taylor in view of Lyke et al.

The embodiments disclosed in the present application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, does not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The present invention is generally directed to a semiconductor memory apparatus having a selectable memory capacity and to methods for testing such devices. In an embodiment, as shown in Figure 1 of the present application, configuration circuits 30, 40, 38 are capable of selectively coupling or decoupling address, data or control lines in the processor 102 to lines in a memory device 10. In another embodiment, as shown in Figure 3, a memory device 80 includes a pair of memory dies 82 positioned within a package 84. A configuration circuit 92 is included in the memory device 80 that couples the address pins 86, the data input/output pins 88 and the control pins 90 to the memory dies 82. In a particular embodiment, the configuration circuits includes bi-stable relays 32, and in another embodiment the bi-stable relays may be bi-stable MEMS devices.

The configuration circuits have a closed and an open state and are capable of being configured in either the closed or open state when the circuit is energized by a suitable

source. One aspect of the disclosed embodiment over prior art is that the configuration circuits are non-volatile in the sense that they do not require a constant power source to maintain the selected state once the selected state has been actuated. The selected state of the configuration circuits is maintained independently of a connection to any power source; and therefore the state is not lost when power is interrupted to the memory device.

One use of the disclosed non-volatile configuration circuit is to reconfigure a packaged device when defects have been detected in the packaged device at step 60, as shown in Figure 2. If defects are detected at step 60, an assessment may be made to determine whether the packaged device is configurable into a marketable form. For example, the reconfiguration may involve the memory capacity being restricted for the device, whereupon it may be segregated and suitably identified as qualified for applications requiring not more than the memory capacity that successfully tested at step 60. Then, if the reconfigured packaged device successfully passes the tests conducted again at step 60, the packaged device is then reconfigured into the desired device at step 64 by applying an appropriate configuration control signal to the packaged device (*see* Figure 2). Therefore, rather than discarding packaged devices with known defects, the packaged devices may be adapted to conform to other product applications by configuring the device so that it utilizes the memory capacity demonstrated to be good. To be usable in this manner, the configuration circuit must, of course, be non-volatile so that the desired configuration will be retained when the packaged device is shipped to a customer.

Another aspect of the disclosed embodiment over prior art is the ability to reconfigure a device package 84 when at least one memory die 82 fails during testing where the device package contains multiple memory dies 82. Typically, the memory dies 82 are interconnected within the package 84 to cooperatively form a memory device 80 having a memory capacity that is approximately the sum of the memory capacities of the dies 82. (*See* Figure 3). For example, if the there are two memory dies 82 that are individually 128 Mb DRAM dies and they are packaged together into one device package 84, the memory capacity of the memory device 80 is then approximately about 256Mb. If one of the memory dies within the package is rejected during testing, generally the entire package will be discarded. However, one aspect of the embodiment disclosed in Figure 3 has the advantage of using a configuration control signal 36 to selectively open or close the configuration circuits. The configuration circuit

92 may be selectively opened or closed by transferring a suitable signal from the external circuits to the configuration circuit 92 through one or more configuration pins 94 that are positioned on the package 84. This allows the packaged device to be salvaged if one of the memory die within the packaged device is rejected during testing and the other tested good. For example, if the packaged device is the 256Mb described above and one of the 128Mb die is rejected and the other is tested good, the packaged device may be configured as a 128Mb device only. Again, the configuration circuit must be non-volatile so that the reconfigured device will retain its configuration when the device is shipped to a customer or power is removed from a system containing the packaged device.

The Examiner has cited the Kajimoto et al reference. The Kajimoto et al reference is directed toward solving the problem of increasing the speed of a large-scale integrated circuit device by reducing the length of the data bus by using a by pass circuit BPC when an IC memory device fails. In addition, the Kajimoto et al reference is directed toward using a control repeating buffer CRB and an address repeating buffer ARB to compensate for the attenuation in level of control signal and address signals, respectively. Typically, a repeating buffer, CRB and ARB, or a bypass circuit BPC is a logic circuit that requires a constant power source to maintain the selected state. Furthermore, the reference does not suggest that the repeating buffers, CRB and ARB, and the bypass circuit BPC are nonvolatile, and it certainly does not suggest any specific non-volatile device, such as a bi-stable relay device or a MEMS relay. In fact, the example of the bypass circuit shown in Figure 1 is composed of standard logic gates, which, of course, are normally volatile. Therefore, the Kajimoto et al reference does not disclose or fairly suggest using a non-volatile configuration circuit that once the selected state is actuated, a constant power source is no longer required in order to maintain the selected state. Nor does it suggest the desirability of using a non-volatile configuration circuit in place of a volatile configuration circuit.

The Examiner has also cited the Taylor reference. The Taylor reference is directed toward eliminating cross talk and decreasing signal noise on the control, address and data busses. Cross talk and signal noise is caused by magnetic fields interfering with one another. They are minimized by spacing conductors farther from each other and from other electrical components. The Taylor reference applies optical signals, rather than electrical

signals, to transmit control, address and data bits in order to prevent cross talk. Figure 3 of the Taylor reference shows a plurality of memory devices 304-310, in which each memory device receives two corresponding optical chip select bits CS1#-CS2# configured to an external memory controller. The memory controller 312 activates one chip select bit CS1#-CS2# at a time, and this activates the memory device. Typically, a memory controller requires a constant power source to maintain the activated state. Therefore, the Taylor reference does not disclose or fairly suggest using a non-volatile configuration circuit that once the selected state is actuated, a constant power source is no longer required in order to maintain the selected state.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Presently amended independent claim 1 recites, in part, "[a] computer system, comprising:...*at least one bi-stable relay device* interposed between at least one of the address, control and data buses of the processor and the respective address, control and data buses of the memory device to selectively couple lines in at least one of the address, control and data busses of the processor to lines in at least one of the address, control and data busses of the memory device." (Emphasis Added). The Kajimoto et al reference does not disclose using the limitation of a bi-stable relay. In fact, as alluded to above, the Kajimoto et al reference refers to using a bypass circuit BPC or repeating buffers, CRB and ARB, which typically require a constant power source to maintain the selected state. The Kajimoto et al reference does not suggest or imply that the bypass circuit BPC or repeating buffers, CRB and ARB, are nonvolatile. In contrast, the presently amended independent claim 1 includes the limitation of a bi-stable relay, and bi-stable relays do not require a constant power source to maintain the selected state. Therefore, presently amended independent claim 1 is allowable over the Kajimoto et al reference.

Turning now to claim 14, presently amended independent claim 14 recites, in part, "[a] memory device, comprising:...a *non-volatile* configuration circuit interposed between the memory cell array and the one or more signal busses of the external device to selectively couple portions of the one or more busses to the memory cell array, *the non-volatile configuration circuit operable to maintain a selected state independent of a connection to a power source*." (Emphasis Added). The Kajimoto et al reference does not disclose or fairly suggest this limitations. In fact, as explained above with respect to claim 1, the Kajimoto et al

reference does not suggest or imply that the bypass circuit or the repeating buffers are nonvolatile. In contrast, the presently amended independent claim 14 does not require a constant power source to maintain the selected state. Therefore, presently amended independent claim 14 is allowable over the Kajimoto et al reference.

Presently amended independent claim 22 recites, in part, "a *non-volatile* configuration circuit operable to couple either or both of the first memory die and the second memory die to external circuits to selectively obtain a memory device having a third memory capacity, *the non-volatile configuration circuit operable to maintain a selected state independent of a connection to a power source."* (Emphasis added). The Taylor reference does not disclose or fairly suggest the above limitation. Rather, as alluded to above, the Taylor reference refers to a memory controller which functions to access the individual memory devices and does not suggest that or even imply that the memory controller is nonvolatile. In contrast, presently amended independent claim 22 has a non-volatile configuration circuit that is capable of reconfiguring the package. The selected state of the reconfiguration is maintained independently from a connection to a power source. Therefore, presently amended independent claim 22 is allowable over the Taylor reference.

The Examiner has also cited the Lyke reference and the McKeon reference. The Examiner cited a rejection under 35 U.S.C. 103(a) over the Kajimoto et al reference in view of McKeon for claims 2, 11, and 15 and Lyke for claims 3, 16, and 17. The McKeon and Lyke references do not make up for the limitations found in presently amended independent claims 1 and 14, which was not disclosed in the Kajimoto et al reference as referred to above. Therefore, claims depending from claim 1 and 14 are allowable over the Kajimoto et al reference in view of McKeon and Lyke.

The Examiner cited a rejection under 35 U.S.C. 103(a) over the Taylor reference in view of a McKeon reference for claims 23-26 and 28 and a Lyke et al reference for claim 27. In view of the provisions of 35 U.S.C. 103(c), the Taylor reference may not be used as a reference in a rejection under 35 U.S.C. 103(a). The Taylor reference may not be properly used in a 35 U.S.C. 103(a) rejection because it is a reference under 35 U.S.C. 102(e)(1) and the Taylor reference and the present application were commonly owned by Micron Technology Inc. at the

time the present invention was made. Accordingly, the Taylor reference is disqualified as a reference under 35 U.S.C. 103(a) in view of 35 U.S.C. 103(c).

The claims depending from the above-discussed independent claims are also patentable because of their dependency from patentable independent claims and because of the additional limitations recited in the dependent claims.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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